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|-----------------------------|-------------------|
| <b>Application Number</b>   | 10/643,050        |
| <b>Filing Date</b>          | 08/18/03          |
| <b>First Named Inventor</b> | James H. Kukula   |
| <b>Art Unit</b>             | 2825              |
| <b>Examiner Name</b>        | ROSSOSHEK, YELENA |

Attorney Docket Number

SNPS 0504

**NON PATENT LITERATURE DOCUMENTS**

| Examiner Initials* | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.  | T <sup>2</sup> |
|--------------------|-----------------------|--|----------------|
|                    | 1                     | "Representing circuits more efficiently in symbolic model checking." Burch, J.R.; Clarke, E.M.; Long, D.E. ACM/IEEE 28th Design Automation Conference, 1991. Publication Date: June 17-21, 1991. On page(s): 403 – 407.  |                |
|                    | 2                     | "Efficient Model Checking by Automated Ordering of Transition Relation Partitions." Daniel Geist , Ilan Beer. Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23, 1994. On page(s): 299-310.   |                |
|                    | 3                     | "Early quantification and partitioned transition relations." Hojati, R.; Krishnan, S.C.; Brayton, R.K. Proceedings, IEEE International Conference on Computer Design (ICCD): VLSI in Computers and Processors, 1996. Publication Date: 7-9 Oct. 1996. On page(s): 12 - 19.                                     |                |
|                    | 4                     | "Border-Block Triangular Form and Conjunction Schedule in Image Computation." In-Ho Moon , Gary D. Hachtel , Fabio Somenzi. Proceedings of the Third International Conference on Formal Methods in Computer-Aided Design. Publication Date: November 01-03, 2000. On page(s): 73-90.                           |                |
|                    | 5                     | "Efficient BDD algorithms for FSM synthesis and verification." R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixley. International Workshop for Logic Synthesis, May 1995. Lake Tahoe, CA.  |                |
|                    | 6                     | "Implicit state enumeration of finite state machines using BDD's." Touati, H.J., Savoj, H., Lin, B., Brayton, R.K. and Sangiovanni-Vincentelli, A. IEEE International Conference on Computer-Aided Design (ICCAD), 1990. Digest of Technical Papers. Publication Date: 11-15 Nov. 1990. On page(s): 130 – 133. |                |
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Examiner Signature

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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